REMARKS

Claims 1-25 were originally filed in the present application.

Claims 1-25 were previously cancelled.

Claims 26-49 were previously added.

Claims 26-49 are pending in the present application.

Claims 26-49 were rejected in the July 26, 2006 Office Action.

No claims have been allowed.

Claims 26 and 38 are amended herein

Claims 26-49 remain in the present application.

Reconsideration of the claims is respectfully requested.

In Sections 3 and 4 of the July 26, 2006 Office Action, the Examiner rejected Claims 26-49 under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter that the Applicant regards as the invention. Specifically, the Examiner pointed to a lack of antecedent basis for the term "the value" in Claims 26 and 38. In response, the Applicant has amended Claims 26 and 38 to recite "a value." The Applicant respectfully requests the withdrawal of the rejection under § 112, second paragraph.

In Sections 5-17 of the Office Action, the Examiner rejected Claims 26-49 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,222,220 to *Mehta* (hereafter, "Mehta") in view of U.S. Patent No. 5,535,329 to *Hastings* (hereafter, "Hastings"). The Applicant respectfully traverses the rejection.

In rejecting independent Claims 26 and 38, the Examiner acknowledged that Mehta does not teach storing a first predetermined value in a first address location immediately preceding a range of memory encompassed by a stack. However, the Examiner asserted that Mehta shows comparing a value in "the first address location" to the first predetermined value, to determine if a stack operation corrupted the first predetermined value stored in "the first address location," citing Mehta's description of reading a return address from the stack in an RTS or RTI instruction and comparing the return address to an address stored in a return address latch register. The Applicant respectfully submits that the Examiner misapplied the teaching of Mehta to the language of the claims.

The "first address location" referred to in the comparing step of Claim 26 is a location immediately preceding the range of memory encompassed by the stack. In contrast, the return address read by the RTS or RTI instruction of Mehta is read from a location within the stack. As such, Mehta teaches comparing a value read from a location within the stack to a second copy of the data originally stored in the location, rather than describing comparing a value in a location preceding the stack to a predetermined value.

The Applicant submits that Hastings does nothing to overcome the shortcomings of Mehta. Hastings teaches maintaining a memory status array with entries describing a status of memory locations and, prior to an operation that writes to or reads from a memory location, signaling an error if the location's status value in the status array indicates that the planned memory operation would be inappropriate. (See, Hastings, col. 9, lines 22-61). Thus, Hastings does not teach detecting the occurrence of a stack operation, but rather the impending performance of a memory operation.

Furthermore, the Examiner asserted that Hastings, in the Abstract and at column 11, lines 41-67, describes storing a predetermined value in a location immediately preceding a range of memory encompassed by a stack. The Applicant respectfully submits that the Examiner mischaracterized the teaching of Hastings.

In the cited passage, Hastings describes storing special 8 byte values in locations before and after arrays in the heap, data and 'bss' segments of memory. The data and 'bss' segments are located in region 300 of Figure 7 and the heap is located in region 400 of Figure 7. (See, Hastings, col. 10, lines 6-10). The stack is located in region in region 500 of Figure 7. (See, Hastings, col. 10, lines 13-14). An examination of Figure 7 shows that region 500 is not adjacent to regions 300 and 400. Thus, Hastings' description of storing values in memory located in regions 300 and 400 does not describe storing a first predetermined value in a first address location immediately preceding a range of memory encompassed by a stack, as recited in Claims 26 and 38.

For these reasons, independent Claims 26 and 38 are patentable over the cited references. Claims 27-37 and 39-49 depend from Claims 26 and 38, respectively, and include all the limitations of their respective base claims. Therefore, Claims 27-37 and 39-49 also are patentable over the cited references. As such, the Applicant respectfully requests that the rejection under § 103 be withdrawn.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of the pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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